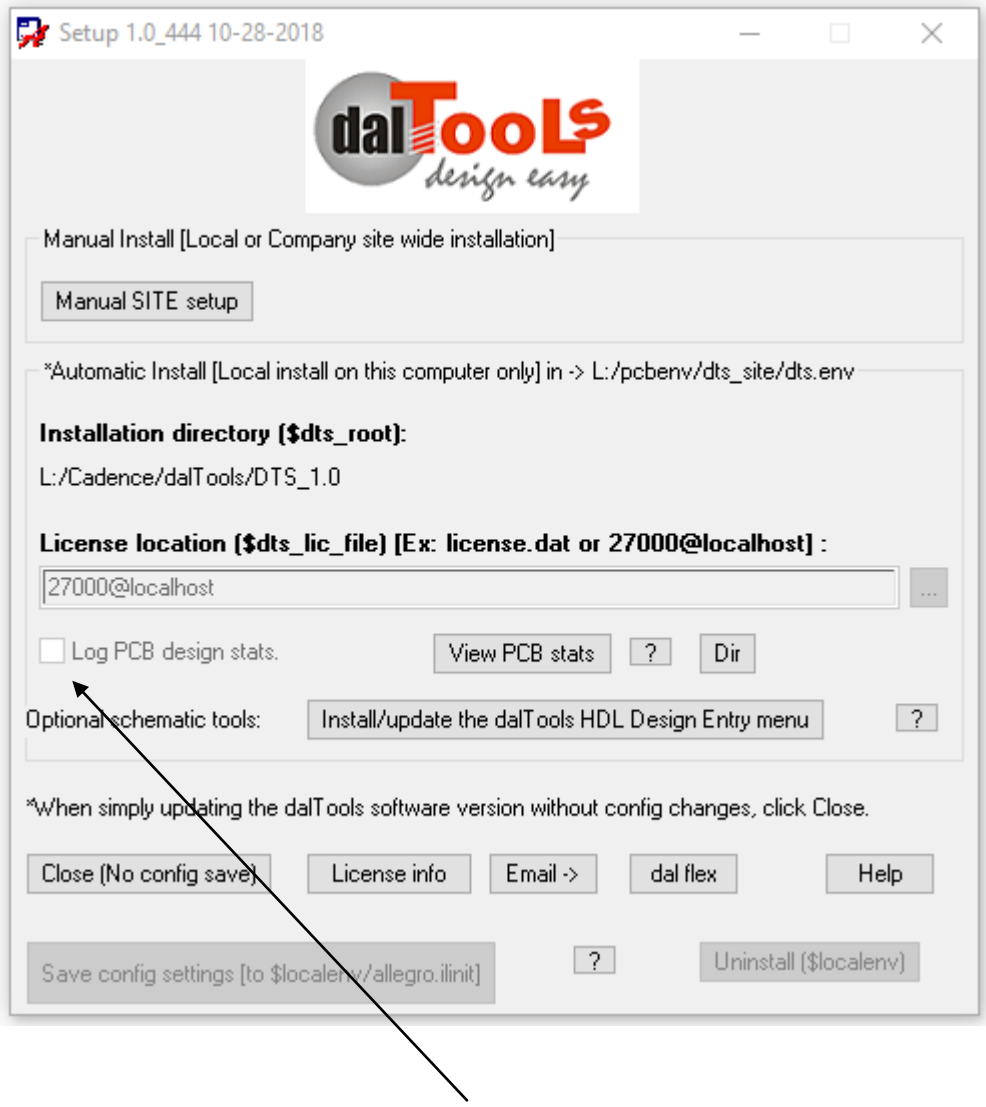
PcbStat

Automatically records and reports PCB Design related statistics and data for all PCB Layouts. Information captured and summarized is: Total editing time, drcs, placed symbols, etc.

Features:

- ❑ This document is currently incomplete.



When the “Log PCB design stats. button is checked, the PCB layout status of every design (.brd,.mcm,.sip,.dra) will be logged in the directory specified by the variable "dts_pcbstat_dir" as set in the allegro.ilinit, dts.env or pcbenv/env file.

See the ../dts_site/dts.env file for details if you would like to change the default location.

This file is automatically appended to upon each save or exit from an Allegro database.

This is an example of what the report looks like: jdoe.csv

OB Date,Design ID,OB ID,DRC Count,DRC State,Placed,Total Components,Connections,Connected,Nets,NOTEST,TPOINTS,Reg Hours,OT Hours,Editing Time,Login Name,Board Name,Computer Name,CDS Version

Sep 18 22:50:50 2017,0,0,12,TBD,0,0,0,0,0,0,0,0.000000,0.000000,0.000000,dlocke,test.brd,DLOCKEHOME,17.2-2016 S025