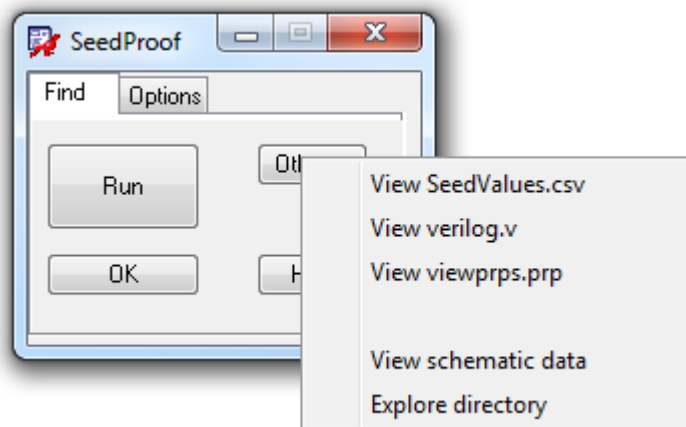
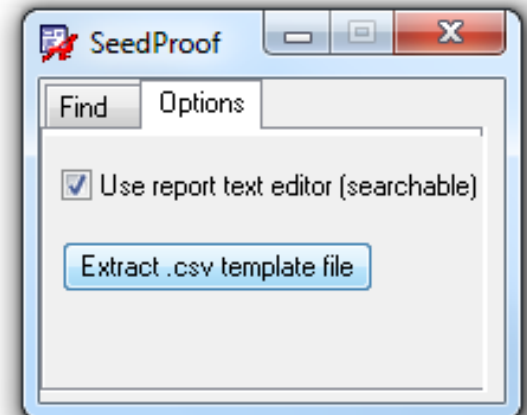
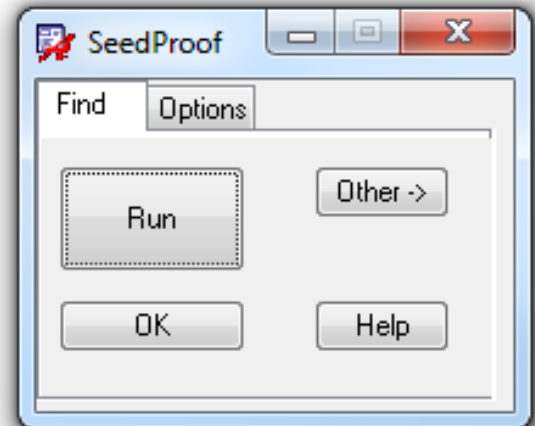


## HdlSeedProof

Verifies an excel spreadsheet of master seedjob refdes, pin numbers and signal names versus what exists in the HDL schematic database. Optionally updates the pin values and sig\_name properties to match the master seed job spreadsheet.

Features:

- ❑ Automatic pin\_value and signame renaming preventing typos.
- ❑ Comprehensive report of mismatches with option to fix.
- ❑ Comment lines in the .csv file may start with #.
- ❑ Extracts a seed job .csv file from the active schematic.
- ❑ Reports are saved as unique file names based on the date and time.



# Example 1

SeedValues.csv

```
1 REF DES, PIN, NUMBER, VALUE
2 #P1, 1, TEST2
3 P114, A1, CBIT0
4 P114, B1, CBIT1
5 P111, A1, CBIT16
6 P106, J3, I2CCLK0
7 P106, I4, I2CDATA0
8 #P303, 19, F_OUT_5_C
9 #P303, 2, F_IN_4
10 #P216, B4, GPOUT1
11 #P216, A4, GPIN1
12
13
14 P302, 18, S_OUT_2_A
15 P301, 4, F_IN_1
16 P301, 17, F_OUT_1_B
17 P112, B5, APU12_30_35_FL
18 P112, C6, APU12_34S
19 P112, D7, APU12_28F
20 P113, D8, APU12_22F
```

```
1 REFDES, SCHPIN, PINVALUE, NETNAME, XY, PRTPIN, SYMNAME, PATH, PAGE
2 P114, B5, +12V, +12V, (-750, 1900), 1, ETS600_POGO_143P, I11, 10
3 P106, B5, +12V, +12V, (-750, 2100), 1, ETS600_POGO_143P, I9, 10
4 P103, B5, +12V, +12V, (-750, 2200), 1, ETS600_POGO_143P, I8, 10
5 P111, B5, +12V, +12V, (-750, 2000), 1, ETS600_POGO_143P, I10, 10
6 P103, G4, +15V, +15V, (-850, -300), 1, ETS600_POGO_143P, I57, 10
7 P103, F2, +15V, +15V, (-850, 0), 1, ETS600_POGO_143P, I54, 10
8 P103, F3, +15V, +15V, (-850, -100), 1, ETS600_POGO_143P, I55, 10
9 P103, G3, +15V, +15V, (-850, -200), 1, ETS600_POGO_143P, I56, 10
0 P103, I3, +24V, +24V, (-1700, 2000), 1, ETS600_POGO_143P, I3, 10
1 P103, H2, +24V, +24V, (-1700, 2200), 1, ETS600_POGO_143P, I1, 10
2 P103, H3, +24V, +24V, (-1700, 2100), 1, ETS600_POGO_143P, I2, 10
3 P103, I4, +24V, +24V, (-1700, 1900), 1, ETS600_POGO_143P, I4, 10
4 P111, B9, +5V, +5V, (-750, 750), 1, ETS600_POGO_143P, I41, 10
5 P106, B7, +5V, +5V, (-750, 1050), 1, ETS600_POGO_143P, I36, 10
```

Allegro PCB Design XL



Would you like to automatically update the schematic PIN\_VALUE and SIG\_NAME mismatches?

Yes

No

SEEDPROOFLOG\_Jun\_13\_23\_31\_02\_2012.txt

```
1 ALL VALUES UP TO DATE - NO CHANGES MADE
2
```

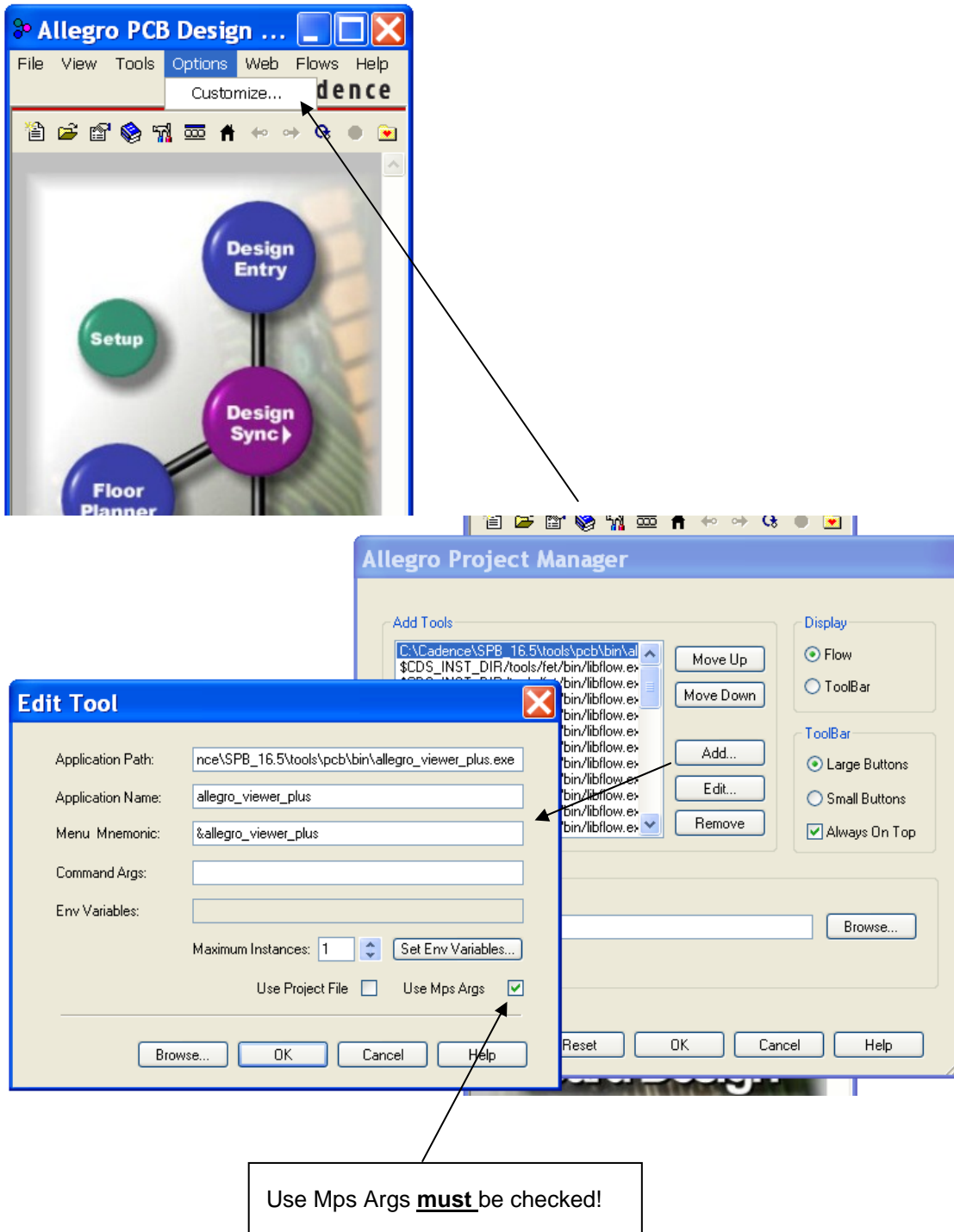
SEEDPROOFLOG\_Jun\_13\_23\_32\_21\_2012.txt

```
1 1 ERROR - REF P1/PIN 1 NOT FOUND IN SCHEMATIC, BUT PRESENT IN EXCEL FILE, PLEASE ADD TO SCHEMATIC
2 2 REF P114/PIN A1 with PIN_VALUE "CBIT0" was updated to "CBIT0_TEST" on page 8 I1 (-3000,3250)
3 3 REF P114/PIN A1 with NET_NAME "CBIT0" was renamed to "CBIT0_TEST" on page 8 I1 (-3000,3250)
4
5 EOF
```

## [Sample reports](#)

# Setup

The seedproof and netplace use the free\_viewer\_plus license so they have to be set up correctly in the project manager in order to function properly. Do the following:



# Help

---

